Data Sheet | April 2000 | File Number 2908.5

63MHz, Ultra-Low Noise Precision Operational Amplifier

The HA-5137 operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Intersil Dielectric Isolation technology and advanced processing techniques, this unique design unites low noise $(3nV/\sqrt{Hz})$ precision instrumentation performance with high speed (20V/µs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10µV), wide gain bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

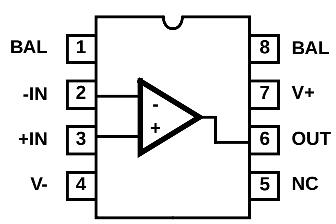
Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. For the military grade product, refer to the HA-5137/883 data sheet.

Pinout

HA-5137A
(CERDIP)
TOP VIEW



Features

- Slew Rate 20V/µs
- Wide Gain Bandwidth ($A_V \geq 5$) 63MHz
- Low Noise. . . . . $3nV/\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10µV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See Application Note AN553

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA7-5137A-5	0 to 75	8 Ld CERDIP	F8.3A

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- Terminals. 44V
Differential Input Voltage (Note 1) 0.7V
Output Current . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5137A-5 . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^oC/W)	θ_{JC} (^oC/W)
CERDIP Package.	115	28

Maximum Junction Temperature (Hermetic Package) . . . . 175^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \le 50pF$, $R_S \le 100\Omega$

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	10	25	μV
		Full	-	30	60	μV
Average Offset Voltage Drift		Full	-	0.2	0.6	μV/^{o}C
Bias Current		25	-	10	40	nA
		Full	-	20	60	nA
Offset Current		25	-	7	35	nA
		Full	-	15	50	nA
Common Mode Range		Full	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)		25	1.5	6	-	MΩ
Input Noise Voltage (Note 4)	0.1Hz to 10Hz	25	-	0.08	0.18	μV_{P-P}
Input Noise Voltage Density (Note 5)	f = 10Hz	25	-	3.5	8.0	$nV/\sqrt{Hz}$
	f = 100Hz	25	-	3.1	4.5	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	3.0	3.8	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5)	f = 10Hz	25	-	1.7	4.0	$pA/\sqrt{Hz}$
	f = 100Hz	25	-	1.0	2.3	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_{OUT} = \pm10V$	25	1000	1800	-	V/mV
		Full	600	1200	-	V/mV
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	114	126	-	dB
Minimum Stable Gain		25	5	-	-	V/V
Gain-Bandwidth-Product	f = 10kHz	25	60	80	-	MHz
	f = 1MHz	25	-	63	-	MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 600\Omega$	25	±10.0	±11.5	-	V
	$R_L = 2k\Omega$	Full	±11.7	±13.8	-	V
Full Power Bandwidth (Note 6)		25	220	320	-	kHz
Output Resistance	Open Loop	25	-	70	-	Ω
Output Current		25	16.5	25	-	mA
TRANSIENT RESPONSE (Note 7)						
Rise Time		25	-	-	100	ns
Slew Rate	$V_{OUT} = \pm3V$	25	14	20	-	V/μs
Settling Time	Note 8	25	-	1.0	-	μs
Overshoot		25	-	20	40	%
POWER SUPPLY CHARACTERISTICS						
Supply Current		25	-	3.5	-	mA
		Full	-	-	4.0	mA

Electrical Specifications V_{SUPPLY} = ±15V, $C_L \leq$ 50pF, $R_S \leq$ 100Ω **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	V_S = ±4V to ±18V	Full	-	2	4	µV/V

NOTES:

3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. The limits for this parameter are based on lab characterization, and reflect lot-to-lot variation.
6. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
7. Refer to Test Circuits section of the data sheet.
8. Settling time is specified to 0.1% of final value for a 10V output step and A_V = -5.

Test Circuits and Waveforms

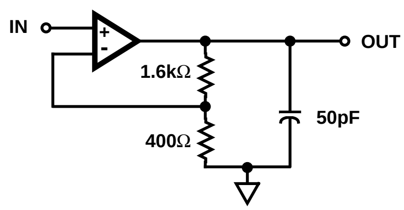
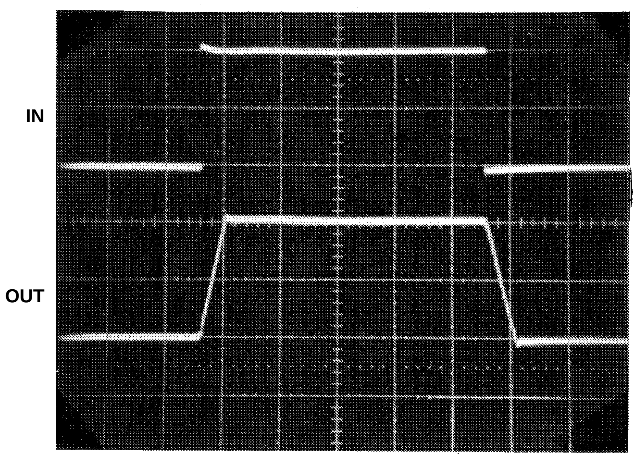
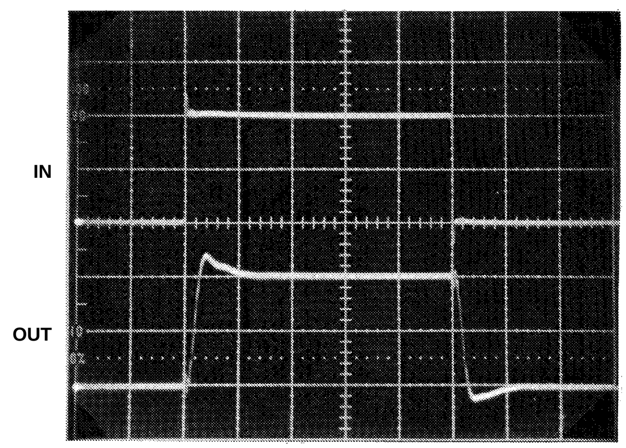


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



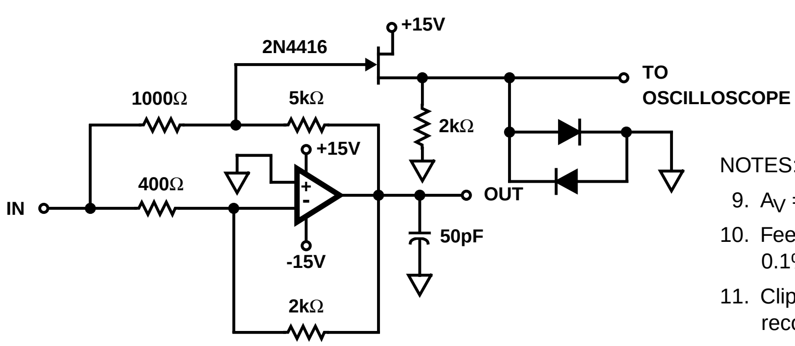
Vertical Scale: Input = 1V/Div.
Output = 5V/Div.
Horizontal Scale: 1µs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: Input = 20mV/Div.
Output = 100mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

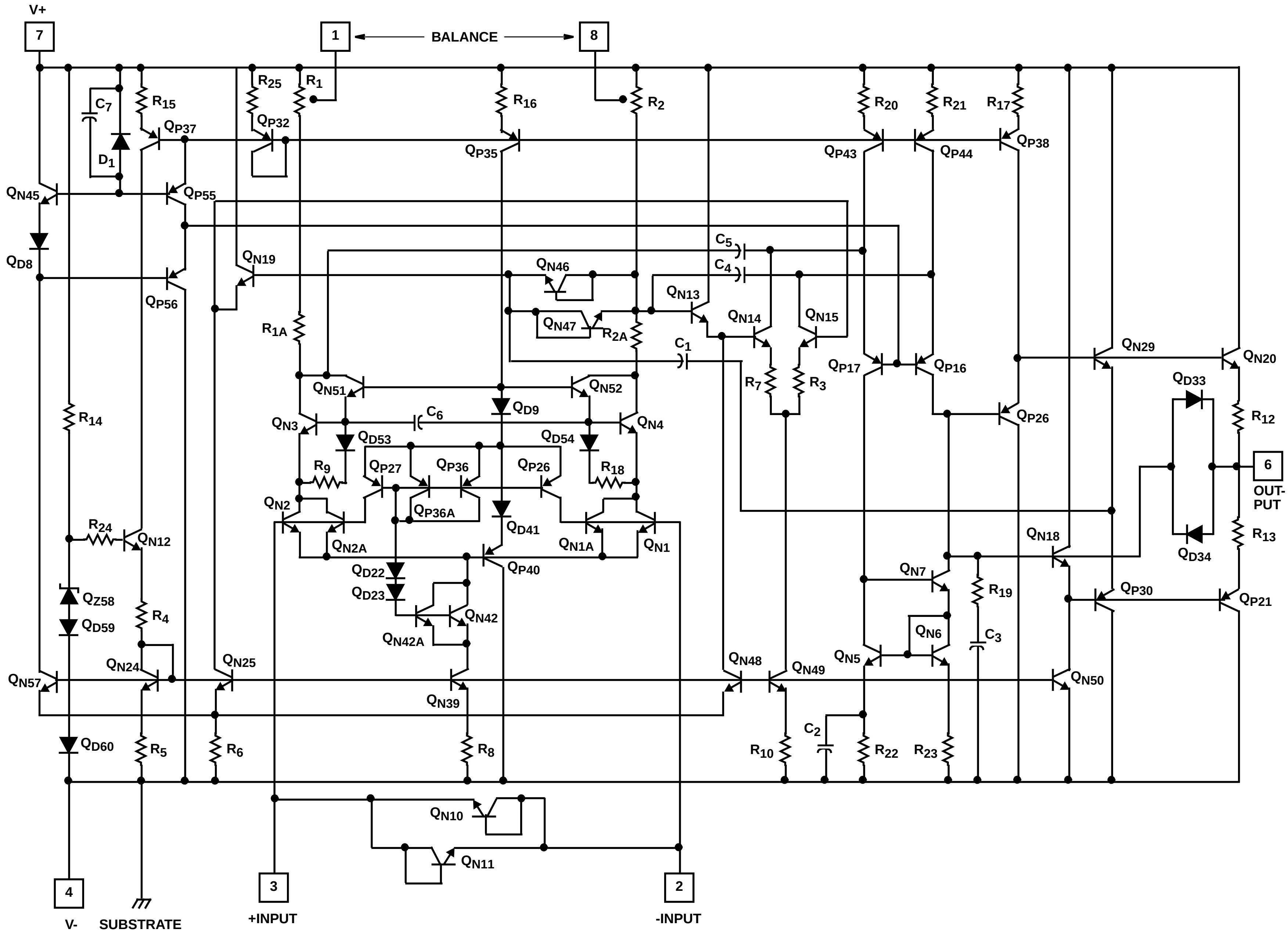


NOTES:

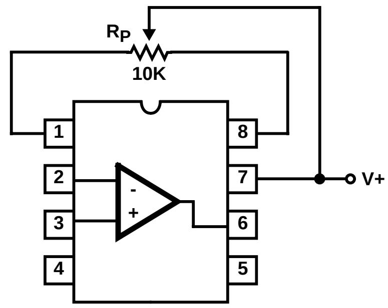
9. A_V = -5.
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram

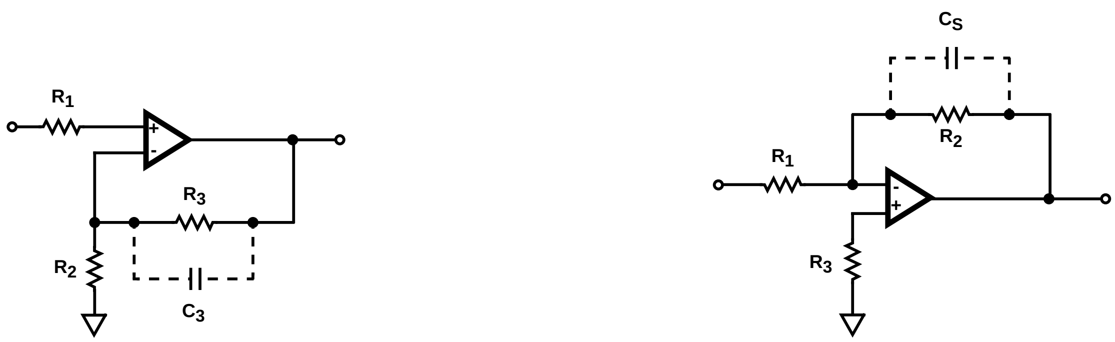


Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±4mV with $R_P = 10k\Omega$.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT



NOTE: Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$

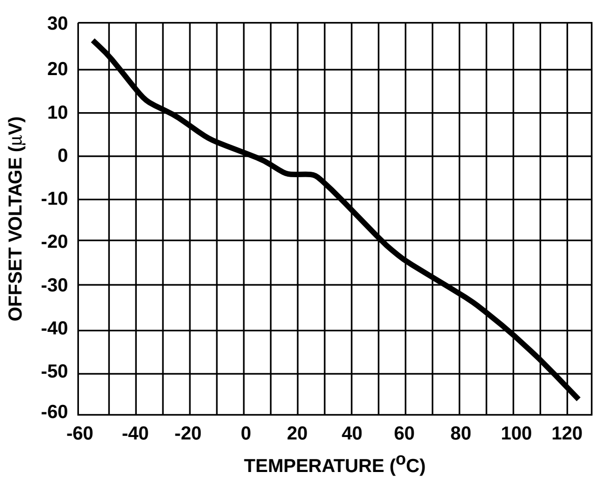


FIGURE 5. OFFSET VOLTAGE DRIFT vs TEMPERATURE

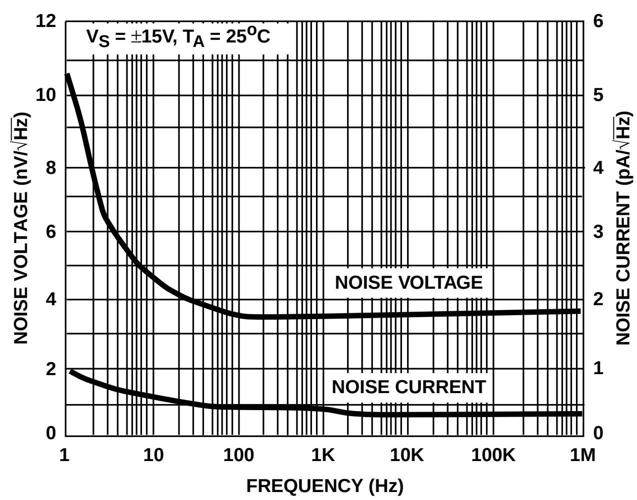


FIGURE 6. NOISE CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$ **(Continued)**

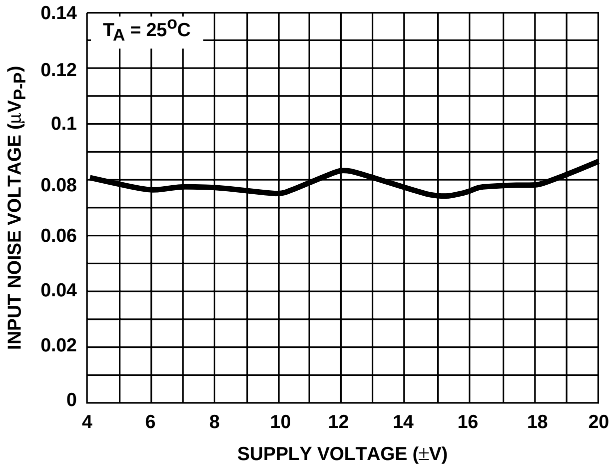


FIGURE 7. NOISE vs SUPPLY VOLTAGE

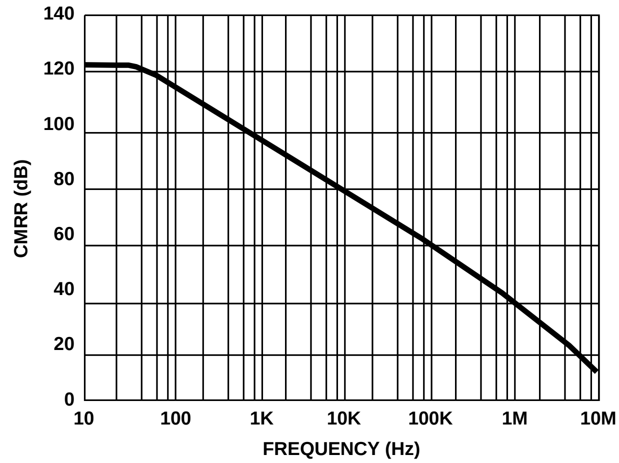


FIGURE 8. CMRR vs FREQUENCY

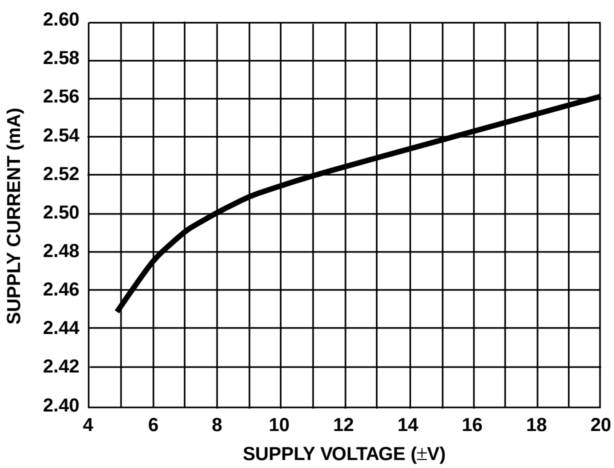


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE

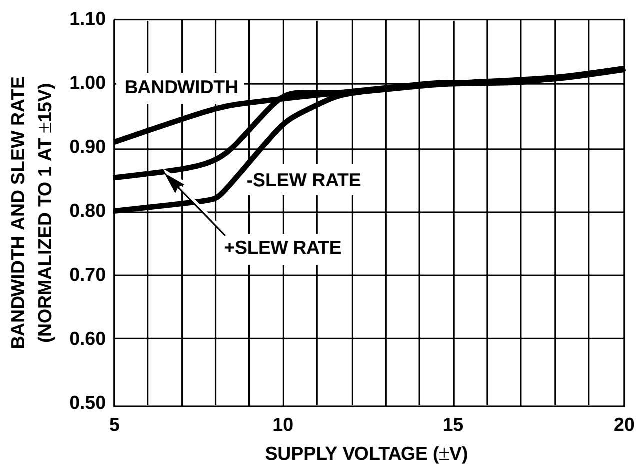


FIGURE 10. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

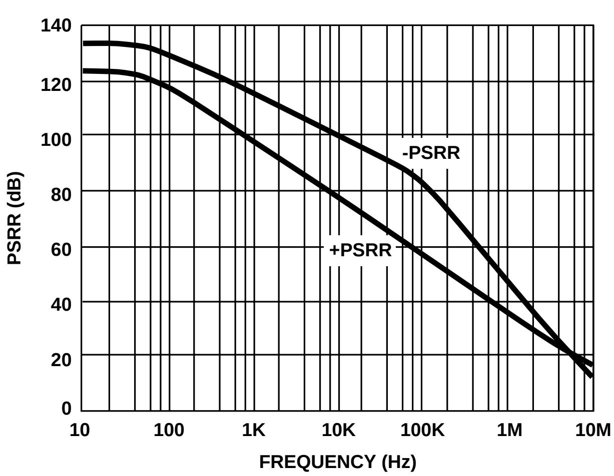


FIGURE 11. PSRR vs FREQUENCY

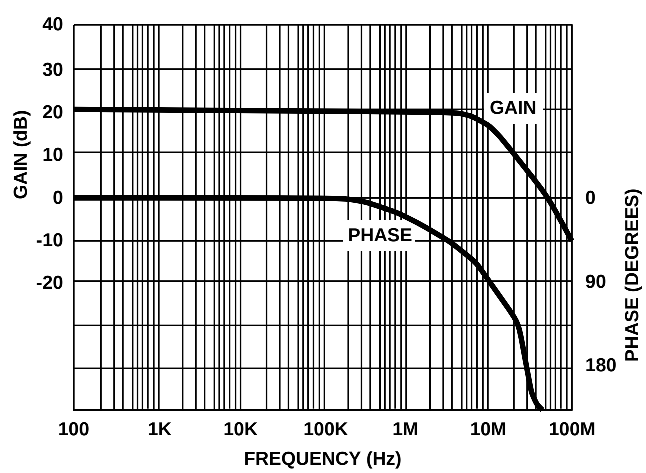


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$ **(Continued)**

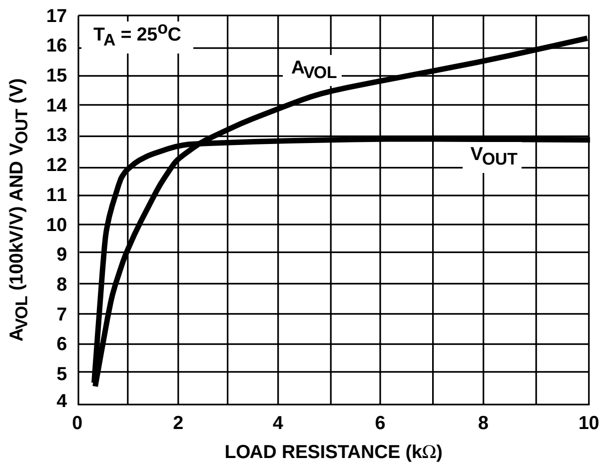


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

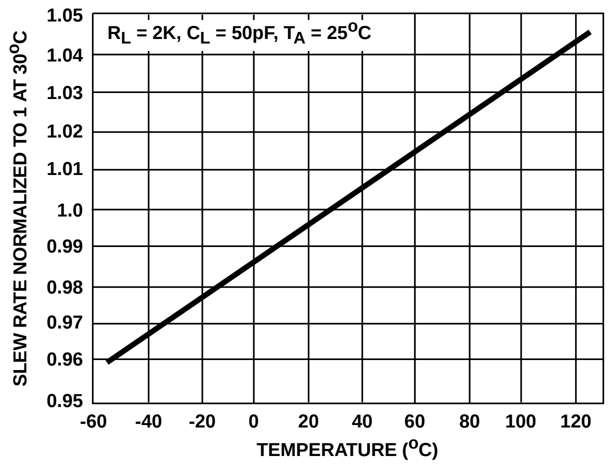


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

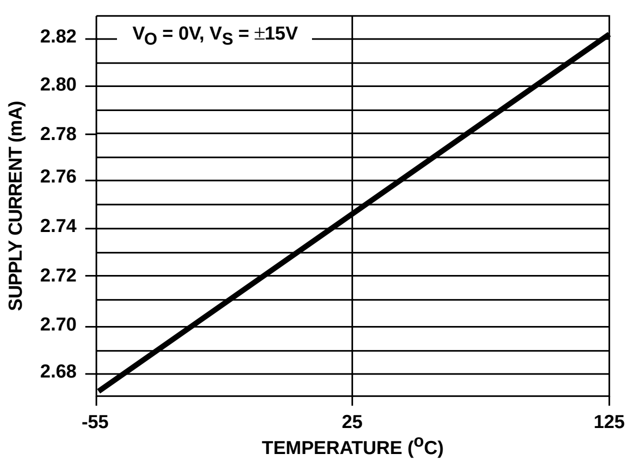


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

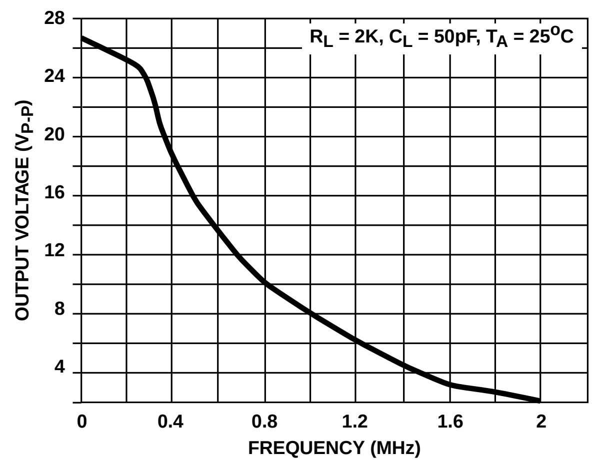


FIGURE 16. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs FREQUENCY

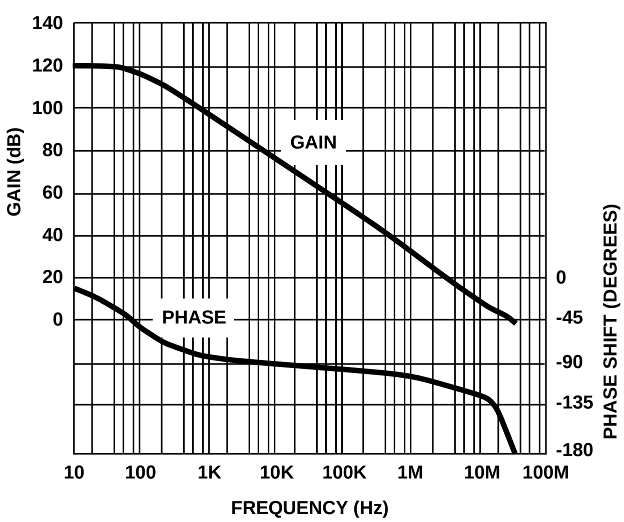
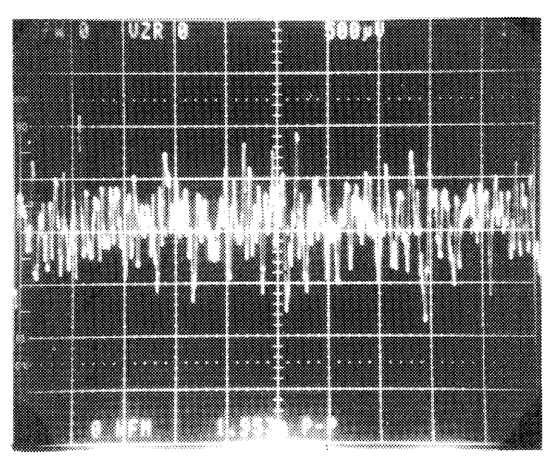


FIGURE 17. OPEN LOOP GAIN AND PHASE vs FREQUENCY



$A_{CL} = 25{,}000V/V$
Horizontal Scale = 1s/Div.
Vertical Scale = 0.002µV/Div., $E_N = 0.08\mu V_{P-P}$ RTI

FIGURE 18. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

Die Characteristics

DIE DIMENSIONS:

104 mils x 65 mils x 19 mils
2650µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (POWERED UP):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

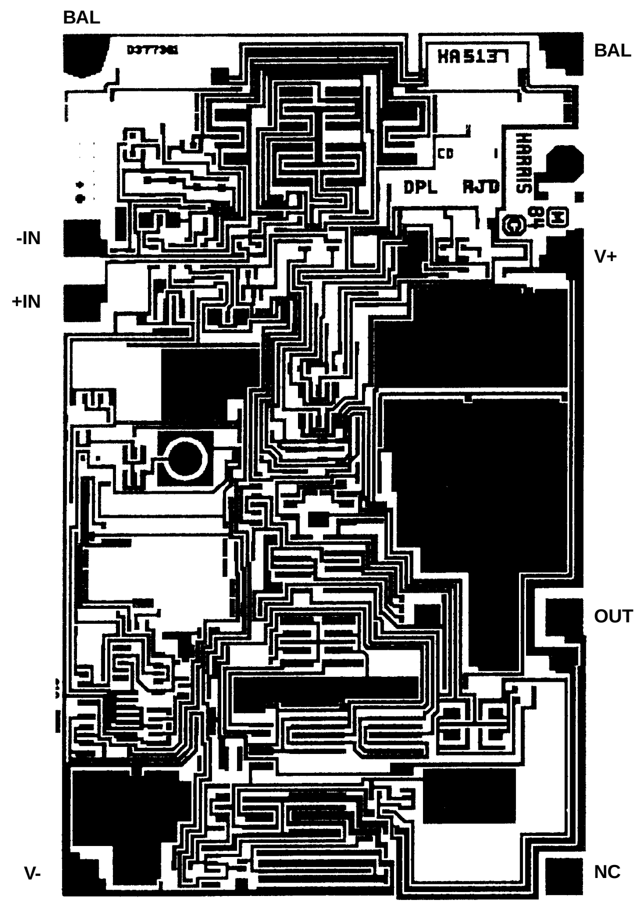
63

PROCESS:

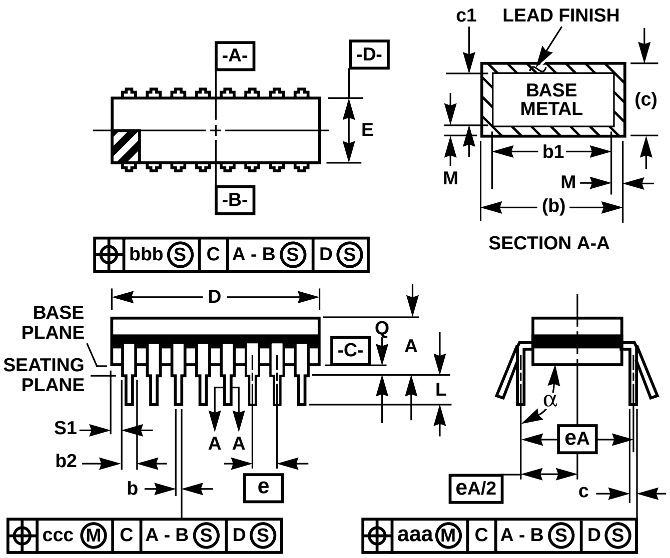
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5137A



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

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